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NTE2057
Integrated Circuit
Dual 16–Bit Digital–to–Analog Converter for CD and DAT Players

Description:

The NTE2057 is a monolithic integrated dual 16–bit digital –to–analog converter (DAC) in a 28–Lead DIP type package designed for use in Hi–Fi digital audio equipment such as compact disc players, digital tape, or cassette recorders.

Features:

- Selectable Input Format: Offset Binary or Two's Complement
- Internal Timing and Control Circuit
- TTL–Compatible Digital Inputs
- High Maximum Input Bit Rate and Fast Settling Time
- 6Mbits/s Data Rate
- Low Linearity Error (1/2 LSB typ)
- Fast Settling (1μs typ)

Applications:

- Compact Disc Players
- Digital Audio Tape, and Cassette Recorders and Players
- Waveform Generation

Absolute Maximum Ratings:

Supply Voltage Range, V_{DD}
- Pin28 (V_{DD}) . . . . . +7V
- Pin26 (V_{DD1}) . . . . . –7V
- Pin15 (V_{DD2}) . . . . . –17V

Junction Temperature Range, T_J . . . . . –55° to +150°C
Operating Ambient Temperature Range, T_A . . . . . –20° to +70°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C
Electrostatic Handling (Note 1), V_{ES} . . . . . –1000 to +1000V

Note 1. Discharging a 250pF capacitor through a 1kΩ series resistor.

DC and AC Electrical Characteristics: (V_{DD} = +5V, V_{DD1} = −5V, V_{DD2} = −15V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply						
Supply Voltage Range Pin28	V_{DD}		4.0	5.0	6.0	V
Pin26	$-V_{DD1}$		4.5	5.0	6.0	V
Pin15	$-V_{DD2}$		14.0	15.0	16.0	V
Supply Currents Pin28	I_{DD}		–	45	60	mA
Pin26	$-I_{DD1}$		–	45	75	mA
Pin15	$-I_{DD2}$		–	25	60	mA
Resolution			–	16	–	bits
Inputs						
Input Current (Pin3, Pin4) Digital Inputs Low	I_{IL}	< 0.8V	–	–	TBD	mA
Digital Inputs High	I_{IH}	> 2.0V	–	–	TBD	μA
Input Frequency At Clock Input (Pin4)	f_{SCK}		–	–	6	MHz
At Clock Input (Pin2)	f_{BCK}		–	–	–	MHz
At Data Inputs (Pin3, Pin4)	f_{DAT}		–	–	–	MHz
At Word Select Input (Pin1)	f_{WS}		–	–	–	kHz
Input Capacitance of Digital Inputs	C_I		–	12	–	pF
Oscillator						
Oscillator Frequency w/Internal Capacitor	f_{OSC}		150	200	250	kHz
Analog Outputs (AOL, AOR)						
Output Voltage Compliance	V_{CC}		TBD	–	TBD	mV
Full−Scale Current	I_{FS}		3.4	4.0	4.6	mA
Zero−Scale Current	$\pm I_{ZS}$		–	TBD	–	nA
Full−Scale Temperature Coefficient	TC_{FS}	T_A = −20° to +70°C	–	±200	–	ppm/°C
Linearity Error Integral	E_1	T_A = +25°C	–	0.5	–	LSB
		T_A = −20° to +70°C	–	TBD	–	LSB
Linearity Error Differential	E_{D1}	T_A = +25°C	–	0.5	1.0	LSB
		T_A = −20° to +70°C	–	TBD	–	LSB
Signal−to−Noise Ratio + THD	S/N	Note 2	90	95	–	dB
Setting Time to ±1 LSB	t_{CS}		–	1	–	μs
Channel Separation	∝		80	TBD	–	dB
Unbalance Between Outputs	ΔI_{FS}		–	0.1	0.2	dB
Time Delay Between Outputs	t_D		–	–	1	μs
Power Supply Ripple Rejection (Note 3)	RR	V_{DD} = +5V	–	TBD	–	dB
		V_{DD1} = −5V	–	TBD	–	dB
		V_{DD2} = −15V	–	TBD	–	dB

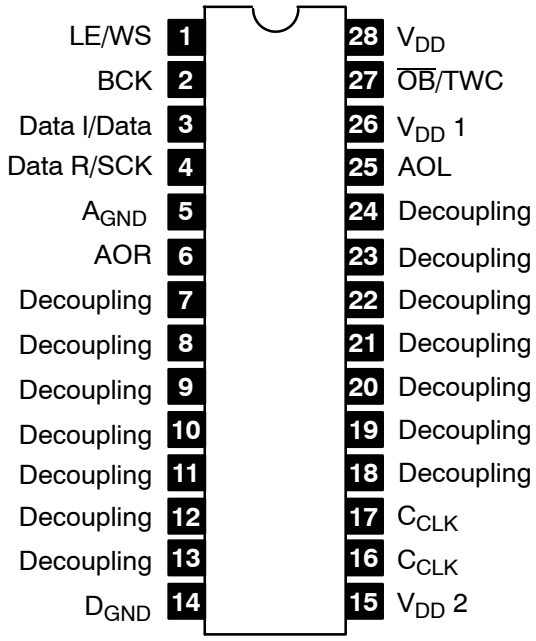
Note 2. Signal−to−noise ratio + THD with 1kHz full−scale sine wave generated at a sampling rate of 176.4kHz.

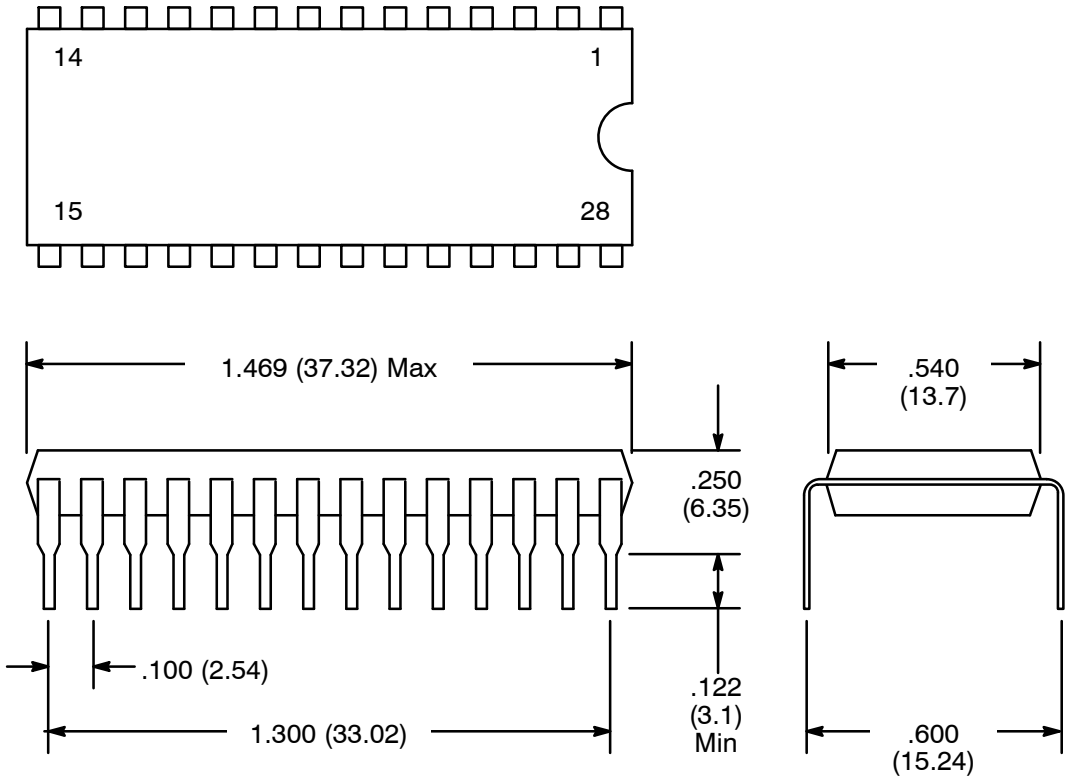
Note 3. V_{RIPPLE} = 1% of supply voltage and f_{RIPPLE} = 100Hz.

DC and AC Electrical Characteristics (Cont'd): (V_{DD} = +5V, V_{DD1} = −5V, V_{DD2} = −15V, T_A = +25°Cunless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Analog Outputs (AOL, AOR) (Cont'd)						
Signal−to−Noise Ratio at Bipolar Zero	S/N		–	−100	–	dB
Timing						
Rise Time	t_R		–	–	35	ns
Fall Time	t_F		–	–	35	ns
Bit Clock Cycle Time	t_{CY}		160	–	–	ns
Bit Clock High Time	t_{HB}		48	–	–	ns
Bit Clock Low Time	t_{LB}		48	–	–	ns
Bit Clock Fall Time to Latch Rise Time	t_{FBRL}		0	–	–	ns
Bit Clock Rise Time to Latch Fall Time	t_{RBFL}		0	–	–	ns
Data Setup Time to Bit Clock	t_{SDB}		32	–	–	ns
Data Hold Time to Bit Clock	t_{HDB}		0	–	–	ns
Data Setup Time to System Clock	t_{SDS}		32	–	–	ns
Word Select Hold Time to System Clock	t_{HWS}		0	–	–	ns
Word Select Setup Time to System Clock	t_{SWS}		32	–	–	ns
Bit Clock Fall Time to System Clock Rise Time	t_{FBRS}		32	–	–	ns
System Clock Rise Time to Bit Clock Fall Time	t_{RSFB}		32	–	–	ns
System Clock Fall Time to Bit Clock Rise Time	t_{FSRB}		50	–	–	ns
Bit Clock Rise Time to System Clock Fall Time	t_{RBFS}		0	–	–	ns
Latch Enable Low Time	t_{LLE}		20	–	–	ns
Latch Enable High Time	t_{HLE}		32	–	–	ns

Pin Connection Diagram




14
1
15
28
1.469 (37.32) Max
.250
(6.35)
.100 (2.54)
1.300 (33.02)
.122
(3.1)
Min
.540
(13.7)
.600
(15.24)