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NTE7227 Integrated Circuit Fixed Multi-Output Positive Voltage Regulator 10-Lead SIP

Description:

The NTE7227 is a multi-output positive voltage regulator in a 10-Lead SIP type package designed to provide fixed precision output voltages of 3.3V & 8V at current up to 0.5A and 5.1V at current up to 1A with an external PNP transistor. An internal reset circuit generates a reset pulse when Output 1 decreases below the regulated value. Output 2 and Output 3 can be disabled by TTL input. Protection features include over voltage protection, short circuit protection and thermal shutdown.

Features:

- Output Currents up to 0.5A (Output 1 & Output 2)
- Output Current up to 1A with External Transistor (Output 3)
- Fixed Precision Output 1 Voltage 3.3V ±2%
- Fixed Precision Output 2 Voltage 8V ±2%
- Control Signal Generator for Output 3 Voltage (5.1V ±2%)
- Reset Facility for Output Voltage 1
- Output 2 and Output 3 with Disable by TTL Input
- Current Limit Protection at Each Output
- Thermal Shutdown

Absolute Maximum Ratings:

DC Input Voltage, V_{IN}	20V
Disable Input Voltage, V_C	20V
Output Current, I_O	0.5A
Power Dissipation (No Heatsink), P_D	1.5W
Junction Temperature, T_J	+150°C
Operating Temperature Range, T_{opr}	0° to +125°C

Electrical Characteristics: ($V_{IN1} = 6V$, $V_{IN2} = 10.5V$, $T_J = +25^\circ C$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
Output Voltage 1	V_{O1}	$6V < V_{IN1} < 14V$	$I_{O1} = 10mA$	3.22	3.3	3.38	V
			$5mA < I_{O1} < 500mA$	3.14	3.3	3.46	V
Output Voltage 2	V_{O2}	$10.5V < V_{IN2} < 18V$	$I_{O2} = 10mA$	7.84	8.0	8.16	V
			$5mA < I_{O2} < 500mA$	7.7	8.0	8.3	V
Dropout Output Voltage	V_{D1}	$I_{O1} = 500mA$	–	–	2.5	V	
	V_{D2}	$I_{O2} = 500mA$	–	–	2.5	V	
Line Regulation	ΔV_{O1}	$I_{O1} = I_{O2} = 200mA$	$6V < V_{IN1} < 14V$	–	–	40	mV
	ΔV_{O2}		$10.5V < V_{IN2} < 18V$	–	–	80	mV
Load Regulation	ΔV_{O1}	$5mA < I_{O1} < 500mA$	–	–	70	mV	
	ΔV_{O2}	$5mA < I_{O1} < 500mA$	–	–	160	mV	
Output Voltage 3	V_{O3}	$V_{SYS} = 7V$, $I_{O3} = 100mA$	4.97	5.1	5.23	V	
Line Regulation	ΔV_{O3}	$13V < V_{IN2} < 18V$, $I_{O3} = 100mA$	–	–	50	mV	
Load Regulation	ΔV_{O3}	$5mA < I_{O3} < 1A$	–	–	110	mV	
Reset Pulse Delay	T_{rd}	$C_D = 100nF$, Note 1	–	25	–	ms	
Saturation Voltage in Reset Condition	V_{rL}	$I_6 = 5mA$	–	–	0.4	V	
Leakage Current at Pin6	I_{rH}	$V_6 = 10V$	–	–	10	μA	
Output Voltage Thermal Drift	ST_t	$0^\circ < T_J < +125^\circ C$, Note 2	–	100	–	ppm/ $^\circ C$	
Short Circuit Output Current	I_{SC1}	$V_{IN1} = 6V$	–	–	1.6	A	
	I_{SC2}	$V_{IN2} = 10.5V$	–	–	1.6	A	
Disable Voltage, High	V_{disH}	Output 2 Active	2	–	–	V	
Disable Voltage, Low	V_{disL}	Output 2 Disabled	–	–	0.8	V	
Disable Bias Current	I_{dis}	$0V < V_{dis} < 7V$	–100	–	2	μA	
Junction Temperature for TSD	T_{tsd}	Note 2	–	145	–	$^\circ C$	
Quiescent Current	I_q	$I_{O1} = 10mA$, Output 2 Disabled	–	–	2	mA	
Reset Threshold Voltage	V_r	$K = V_{O1}$	K-0.4	K-0.25	K-0.1	V	
Reset Threshold Hysteresis	V_{rth}	Note 1	20	50	100	mA	

Note 1. To check the reset circuit, the reset output is low to discharge the delay capacitor ($= C_D$). If it's less than $V_{O1} - 0.25V$. And the reset output is high when the delay capacitor voltage linearly increased by the internal current source ($10\mu A$) if it's more than $V_{O1} - 0.2V$. The equations of delay time is the same as below. $T_{rd} = (C_D \times 2.5) / 10\mu A$.

Note 2. These parameters, although guaranteed, are not 100% tested in production.

Pin Connection Diagram
(Front View)

